

What is claimed is:

1. A logic integrated circuit such as a field programmable gate array having a CPU core:

wherein the CPU core is provided with registers, memories and controller for the registers and memories;

wherein the CPU core has instructions including microcode; and

wherein the controller has control lines for outputting enable signals to the registers and memories, reads in the instruction, and transmits ON/OFF information for each of bits composing microcode included in the instruction to registers and memories allocated to each of the bits, thereby controlling the registers and memories through the directing control lines.

2. The integrated circuit according to claim 1:

wherein the CPU core has address pointer registers in accessing the memories;

wherein the controller has control lines for giving either direction of increment and decrement to the address pointer registers, reads in the instructions, and transmits ON/OFF information for each of bits for giving either direction of increment and decrement to the address pointer registers in microcode included in the instruction through the directing control lines; and

wherein the address pointer registers counts up or counts down values of maintaining addresses when receiving ON information about the bits for giving either direction of increment

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and decrement from the controller through the directing control lines.

3. The logic integrated circuit according to claim 1, wherein the CPU core is further provided with general-purpose registers, and a data transmitting path for connecting the general-purpose registers and memories only through multiplexers for inputting and outputting to and from the general-purpose registers without passing through multiplexers for inputting and outputting memory data, and wherein the CPU core inputs data from the memories to the general-purpose registers with using the data transmitting path.

4. The logic integrated circuit according to claim 1, wherein the CPU core is further provided with general-purpose registers, and a data transmitting path for connecting the general-purpose registers and memories only through multiplexers for inputting and outputting to and from the general-purpose registers without passing through ALU, and wherein the CPU core outputs data to the memories with using the data transmitting path.

5. The logic integrated circuit according to claim 1, wherein the CPU core comprises multiplexers including an integrated interface for inputting data from FIFO that is an accessible memory having data input and output units which are separated from each other, and wherein the CPU core has instructions for reading in data from the FIFO through the multiplexers.

6. A recording medium which is capable of being read out by computers, and records a source as circuit information for composing

a CPU core:

wherein the source is described at hardware description language level for the CPU core on the logic integrated circuit described in claim 1.

7. A logic integrated circuit such as a field programmable gate array having a CPU core:

wherein the CPU core is provided with a program storing memory, a data storing memory, and a controller for controlling the memories and the entire CPU core;

wherein the program storing memory and data storing memory are complete synchronous memories; and,

wherein the controller performs parallel processing in a three-stage pipeline construction, and uses a higher speed clock than normal clocks, thereby reading in data from the program storing memory and data storing memory.

8. The logic integrated circuit according to claim 7, wherein the CPU core is further provided with general-purpose registers, and a data transmitting path for connecting the general-purpose registers and memories only through multiplexers for inputting and outputting to and from the general-purpose registers without passing through multiplexers for inputting and outputting memory data, and wherein the CPU core inputs data from the memories to the general-purpose registers with using the data transmitting path.

9. The logic integrated circuit according to claim 7, wherein the CPU core is further provided with general-purpose registers, and

a data transmitting path for connecting the general-purpose registers and memories only through multiplexers for inputting and outputting to and from the general-purpose registers without passing through ALU, and wherein the CPU core outputs data to the memories with using the data transmitting path.

10. The logic integrated circuit according to claim 7, wherein the CPU core comprises multiplexers including an integrated interface for inputting data from FIFO that is an accessible memory having data input and output units which are separated from each other, and wherein the CPU core has instructions for reading in data from the FIFO through the multiplexers.

11. A recording medium which is capable of being read out by computers, and records a source as circuit information for composing a CPU core:

wherein the source is described at hardware description language level for the CPU core on the logic integrated circuit described in claim 7.

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